IN THE CLAIMS:

1. A method for parallel scrambling of a sequence of serially transmitted digital bits, said method comprising an initializing scrambling step and subsequent scrambling step;
said initializing scrambling step comprising the steps of generating a scrambling bit sequence and storing said scrambling bit sequence in a scrambling register;
and said subsequent scrambling step comprising:

storing a sequential group of bits in the same sequence in which they were received, each of said group of bits containing the same number or fewer bits that said scrambling bit sequence;

XOR-ing said sequential group of bits with corresponding bits of said scrambling bit sequence in parallel, thereby generating scrambled bits;

shifting said bits in said scrambling register by a number of spaces equal to the number of scrambled bits and subsequently transmitting and storing said scrambled bits in corresponding cells of said scrambling register in lowest ordinal sequence for use in subsequent XOR-ing of a next sequential group of bits.

2. A method for parallel scrambling of a sequence of serially transmitted digital bits in accordance with Claim 1, wherein said scrambling bit sequence is comprised of forty three bits.

3. A method for parallel scrambling of a sequence of serially transmitted digital bits in accordance with Claim 1, wherein thirty two bits are processed in parallel.

4. A method for the transmission of digital data in a communication network between any number of transmitters, receivers and transceivers, said method comprising an initializing scrambling step and subsequent scrambling step:

said initializing scrambling step comprising the steps of generating a scrambling bit sequence and storing said scrambling bit sequence in a scrambling register;

and said subsequent scrambling step comprising:

storing a sequential group of bits in the same sequence in which they were received, each of said group of bits containing the same number or fewer bits than said scrambling bit sequence;

XOR-ing said sequential group of bits with corresponding bits of said scrambling bit sequence in parallel, thereby generating scrambled bits;

shifting said scrambling register by a number of spaces equal to the number of scrambled bits and subsequently transmitting and storing said scrambled bits in corresponding cells of said scrambling register in lowest ordinal sequence for use in subsequent XOR-ing of a next sequential group of bits.

5. A method for parallel scrambling of a sequence of serially transmitted digital bits in accordance with Claim 4, wherein said scrambling bit sequence is comprised of forty three bits.

6. A method for parallel scrambling of a sequence of serially transmitted digital bits in accordance with Claim 4, wherein thirty two bits are scrambled in parallel.

7. A method for parallel descrambling of a sequence of serially transmitted digital bits, said method comprising an initializing descrambling step and subsequent descrambling step;

said initializing descrambling step comprising the steps of generating a descrambling bit sequence identical to said scrambling sequence, and storing said descrambling bit sequence in a descrambling register;

and said subsequent descrambling step comprising:

storing a sequential group of bits in the same sequence in which they were received, each of said group of bits containing the same number or fewer bits than said descrambling bit sequence;

XOR-ing said sequential group of bits with corresponding bits of said descrambling bit sequence in parallel, thereby generating descrambled bits;

shifting said descrambling register by a number of spaces equal to the number of descrambled bits and subsequently transmitting and storing said scrambled bits in corresponding

cells of said descrambling register in lowest ordinal sequence for use in subsequent XOR-ing of a next sequential group of bits.

8. A method for parallel descrambling of a sequence of serially transmitted digital bits in accordance with Claim 7, wherein said descrambling bit sequence is comprised of forty three bits.

9. A method for parallel descrambling of a sequence of serially transmitted digital bits in accordance with Claim 7, wherein thirty two bits are descrambled in parallel.

10. A method for the reception of digital data in a communication network between any number of transmitters, receivers and transceivers, said method comprising an initializing descrambling step and subsequent descrambling step:

said initializing descrambling step comprising the steps of generating a descrambling bit sequence and storing said descrambling bit sequence in a descrambling register;

and said subsequent descrambling step comprising:

storing a sequential group of bits in the same sequence in which they were received, each of said group of bits containing the same number or fewer bits than said descrambling bit sequence;

XOR-ing said sequential group of bits with corresponding bits of said descrambling bit sequence in parallel, thereby generating descrambled bits;

shifting said descrambling register by a number of spaces equal to the number of descrambled bits and subsequently transmitting and storing said descrambled bits in corresponding cells of said descrambling register in lowest ordinal sequence for use in subsequent XOR-ing of a next sequential group of bits.

11. A method for parallel descrambling of a sequence of serially transmitted digital bits in accordance with Claim 10, wherein said descrambling bit sequence is comprised of forty three bits.

12. A method for parallel descrambling of a sequence of serially transmitted digital bits in accordance with Claim 10, wherein thirty two bits are descrambled in parallel.

13. A system for the repeated parallel scrambling of a sequence of a first number of serially transmitted input bits, said system being connected to:

- a source of serially transmitted bits;

said system comprises:

- an input register comprising a first number of cells for storing a sequence of bits in the same sequence in which they were received;

- a scrambling register comprising at least a second number of cells, said second number being higher than the number of bits in said received group, for storing at least said second number of scrambling bits, wherein initially:

- a second number of bits is loaded into said scrambling register, and

subsequently:

- each scrambling bit is a scrambled bit preceding the bit to be scrambled by it, by said second number;

- two or more **[a first number of]** XOR gates for the parallel scrambling of said first number of input bits, having two inputs and one output each, wherein:

- one XOR gate input is correspondingly connected to a cell in said first register;

- second XOR gate input is correspondingly connected to a cell in said scrambling register;

- said one XOR gate output is:

- stored for corresponding sequential transmission to a receiver;

- stored for subsequent use in said scrambling register for scrambling a next input bit separated from said input bit by said second number of bits;

said system further comprises:

- clock means operatively connected for the enabling and the disabling of data handling operations.

14. A system for the parallel scrambling of a sequence of serially transmitted digital bits according to claim 13 wherein said first number is thirty two.

15. A system for the parallel scrambling of a sequence of serially transmitted digital bits according to claim 13 wherein said second number is forty three.

16. A system for the repeated parallel descrambling of a sequence of a first number of serially transmitted input scrambled bits, said system being connected to:

- a source of serially transmitted scrambled bits;

said system comprises:

- an input register comprising a first number of cells for storing a sequence of scrambled bits in the same sequence in which they were received;

- a descrambling register comprising at least a second number of cells, said second number being higher than the number of bits in said received group, for storing at least said second number of descrambling bits, wherein initially:

- a second number of bits is loaded into said descrambling register, and

subsequentially:

- each descrambling bit is a scrambled bit preceding the bit to be descrambled by it, by said second number;

- two or more **[a first number of]** XOR gates for the parallel descrambling of said first number of input bits, having two inputs and one output each, wherein:

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one XOR gate input is correspondingly connected to a cell in said first register;

- second XOR gate input is correspondingly connected to a cell in said descrambling register;

- said one XOR gate output is:

- stored for corresponding sequential transmission to a receiver;

- stored for subsequent use in said descrambling register for descrambling next input bit separated from said input bit by said second number of bits;

said system further comprises:

- clock means operatively connected for the enabling and the disabling of data handling operations.

17. A system for the parallel descrambling of a sequence of serially transmitted digital bits according to claim 16 wherein said first number is thirty two.

18. A system for the parallel descrambling of a sequence of serially transmitted digital bits according to claim 13 wherein said second number is forty three.

19. A system for the parallel descrambling of a sequence of serially transmitted digital bits according to claim 16 wherein said first number is thirty two..

20. A system for the parallel descrambling of a sequence of serially transmitted digital bits according to claim 16 wherein said second number is forty three.

21. A method in accordance with claim 1 wherein:

- one input for each XOR operation is a descrambled bit in a sequence of descrambled bits,

- a second input for each XOR operation is a scrambled bit of said sequence, preceding said descrambled bit by forty three bits.

- the output of each one of said XOR operation is a scrambled bit in a sequence of scrambled bits.

22. A method in accordance with claim 1 wherein:

- one input for each XOR operation is a scrambled bit in a sequence of scrambled bits,

- a second input for each XOR operation is a scrambled bit of said sequence, preceding said scrambled bit by forty three bits.

- the output of each one of said XOR operation is an descrambled bit in a sequence of descrambled bits.